What is Claimed is:

1. In a test and debug system in which a target processor transmits trace data to a host processing unit; apparatus for transferring the data from the target processor comprising:

a trace packet unit, the trace packet unit reformatting trace packets into export trace packets; and

a flush packet unit, the flush packet unit generating a flush export trace packet when the trace packet unit does not have sufficient data to generate a trace export packet.

2. Apparatus as recited in claim 1 wherein the flush packet unit is activated in response to a halt signal during a non-interruptible code segment.

3. Apparatus as recited in claim 2 further comprising a storage unit, the storage unit storing a first signal in response to the halt signal, the first signal activating the flush packet unit.

4. Apparatus as recited in claim 3 wherein the first signal is removed when code execution resumes.

5. Apparatus as recited in claim 4 further comprising:

an export unit for transmitting export trace packets to the host processing unit; and

a switch, the switch determining whether an export trace packet or a flush export trace packet is applied to the export unit.

6. The method of generating export trace packets, the method comprising:

reformatting trace packets into export trace packets; and

generating a flush export trace packet when the data from the trace packets do not provide a complete export trace packet.

7. The method as recited in claim 6 wherein the flush export trace packet is generated after a halt signal is generated during execution of a non-interruptible code segment.

8. The method as recited in claim 7 further comprising:

storing a first signal in a storage unit as a result of a halt signal, the halt signal controlling the generation of the flush export trace packet.

9. The method as recited in claim 8 wherein the first signal is removed when the target processor begins executing code.

10. A target processor comprising:

a processing unit;

a trace unit, the trace unit coupled to the processing unit, the trace unit gathering test and debug data from the processing unit, the trace unit formatting the test and debug data in trace packets; and

a trace export unit, the trace export unit including:

a trace packet unit for converting trace packets to export trace packets; and

a flush packet unit for generating trace packets when the converting a trace packet does not result in a complete export trace packet.

11. The target processor as recited in claim 10 wherein the flush packet unit is activated in response to a halt signal during a non-interruptible code segment.

12. The target processor as recited in claim 11 wherein the trace unit further includes a storage unit, the halt signal resulting in a storage of a first signal in the storage unit, the first signal activating the flush packet unit.

13. The target processor as recited in claim 12 wherein the trace unit further includes a switch, the switch determining whether the trace packet unit or the flush trace unit is transmitted to the host processing unit.

14. The target processor as recited in claim 13 wherein the first signal is removed from the storage unit when the processor begins code execution.